REMARKS

The Examiner is thanked for the interview courteously granted to the undersigned, in connection with the above-identified application. During this interview, the undersigned indicated that the subject matter of claim 30 would be incorporated into claim 29; and based upon this amended claim 29 (including the subject matter of claim 30), differences between the presently claimed invention and the teachings of the applied references were discussed. In particular, it was pointed out to the Examiner that the primary applied reference did not disclose the plasma treatment; and, moreover, did not disclose air vents in the other side of the cavity of the molding die, as in previously considered claim 30. It was also pointed out to the Examiner that Hashimoto disclosed a potting molding process, different than the block molding by injecting resin into the cavity as in the primary applied reference, Tsuruta, and as in the present invention. It was noted that in the paragraph relied on by the Examiner in column 15 of Hashimoto, disclosing activation of surfaces of the substrate and of the semiconductor device with oxygen or argon plasma, this plasma treatment was discussed in connection with use of a potting molding. The undersigned contended that the potting molding is a different process than the block molding and involves different problems, such that the potting molding would be non-analogous art with respect to the block molding as in Tsuruta and as in the present invention. While the Examiner contended during the interview that both Tsuruta and Hashimoto, as well as the present invention, are directed to forming semiconductor packaged devices, the undersigned emphasized that the present claims are directed to a method, not the device formed; and that the potting method was clearly a different technological

process, with different problems, than the block molding. With respect to the differences in problems, it was pointed out to the Examiner that the problem addressed according to the present invention was voids in the resin enclosure formed, due to the flow involved along the surface of the substrate and along the semiconductor device occurring during the block molding, which flow did not occur in the potting method, it being noted that Hashimoto does not discuss any problem of voids, with respect to the potting method, corresponding to the voids addressed in connection with the present method or corresponding to the voids (differently caused voids) addressed in the method of Tsuruta. No agreement was reached during the interview.

Initially, it is noted that Applicants are filing concurrently herewith a Request for Continued Examination (RCE) Transmittal for withdrawing finality of the Office Action mailed June 9, 2003. While the Office Action Summary of this Office Action mailed June 9, 2003, indicates that the Office Action mailed June 9, 2003 is a non-Final action, it is clear from page 4 of this Office Action mailed June 9, 2003 and from discussions with the Examiner, that the Action was a Final Office Action. Accordingly, it is respectfully submitted that the present filing of the RCE Transmittal is proper, and withdrawal of the finality of the Office Action mailed June 9, 2003, and entry of the present amendments as a matter of right, are respectfully requested.

In the present amendments, Applicants have amended claim 29 consistent with discussions during the aforementioned interview, to incorporate therein the subject matter of claim 30. In light of this amendment of claim 29, claim 30 has been cancelled without prejudice or disclaimer, and dependencies of claims 31, 32, 34, 37 and 39 have been amended, such that these claims are now dependent on claim 29.

Moreover, Applicants are adding new claims 55-62 to the application. Claims 55 and 59, dependent respectively on claims 29 and 39, recite that the cavity has additional sides to the two sides, the additional sides also having air vents; and claims 56 and 60, dependent respectively on claims 29 and 39, recite that the cavity has four sides in total, including the two sides opposed to each other and an additional two sides opposed to each other, the four sides forming a quadrilateral, and wherein the additional two sides also have air vents. Note, for example, Fig. 6 and the description in connection therewith in paragraph [0065] on page 18 of Applicants' Substitute Specification submitted with the Preliminary Amendment filed January 28, 2002, in the above-identified application. Claims 57 and 61, dependent respectively on claims 29 and 39, recite that the plasma treatment is performed such that, in the block molding step, voids at positions behind the semiconductor chips in the direction of flow of the resin are dislodged and move in response to the flow of the resin in the block molding step; and claims 58 and 62, dependent respectively on claims 29 and 39, recite that the plasma treatment is performed such that, in the block molding step, voids are dislodged and move in response to the flow of resin in the block molding step. Note the paragraph bridging pages 22-23 ([0075]) of the aforementioned Substitute Specification; see also, for example, claims 49-51.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in the Office Action mailed June 9, 2003, that is, the teachings of the U.S. Patents to Tsuruta, No. 6,200,121, to Hashimoto, No. 5,729,437, and to Ishikawa, No. 5,939,792, under the provisions of 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of manufacturing a semiconductor device as in the present claims, including, inter alia, mounting a plurality of semiconductor chips on a plurality of product forming areas, arranged in a matrix, on the main surface of a substrate; after the mounting step, treating the main surface of the substrate by plasma; after the treating step by plasma, arranging the substrate in a molding die with the plurality of semiconductor chips being positioned in a cavity of the molding die and the plurality of product forming areas facing to the cavity; and after arranging the substrate in the molding die, block molding a resin enclosure by injecting resin into the cavity, with the cavity having two sides opposed to each other, a gate formed on one side, of the two sides, and an air vent formed on the other side of the two sides, and wherein in the block molding step the resin is injected into the cavity from the gate to the air vent. See claim 29.

As will be developed further infra, it is respectfully submitted that the present invention addresses the problem of voids being formed in the resin enclosure particularly at a location behind the semiconductor chips in the direction of flow of the resin during the block molding; and particularly in view of this problem addressed by the present invention and the solution thereto, including, inter alia, the treating step by plasma as well as the molding die used, the references as applied by the Examiner would have neither taught nor would have suggested the present invention as a whole, including the problem addressed and source thereof, and the problem solved, and the specific solution to this problem. In connection therewith, note particularly claims 49-51, 57, 58, 61 and 62.

In addition, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such method as in the present claims, having features as discussed previously, and additionally wherein the cavity has additional sides which also have air vents (see claims 55 and 59); more particularly, wherein the cavity has four sides in total, including the two sides opposed to each other and defined in claim 29, and an additional two sides opposed to each other, the four sides forming a quadrilateral, and wherein the additional two sides also have air vents (see claims 56 and 60).

Furthermore, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such a method of manufacturing a semiconductor device as in the present claims, having features as discussed previously, and moreover wherein the resin enclosure includes a plurality of fillers (see claims 34 and 43), in particular wherein a volume content of the plurality of fillers in the resin enclosure is more than 80 volume percent (see claims 35 and 44), and wherein the plurality of fillers are comprised of silica fillers (see claims 36 and 45). When using a resin sealing material containing a large amount of filler, the problem of voids is even greater; and such problem is avoided according to the present invention, even with use of a resin sealing material containing a large amount of filler, by the process according to the present invention.

Moreover, it is respectfully submitted that the teachings of the applied prior art would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining, dependent claims, having features as discussed previously, and further including (but not limited to) wherein in the treating step by

plasma, impurities remaining on the main surface of the substrate are removed (see claims 31 and 40), or the main surface of the substrate is roughened (see claims 32 and 41); and/or wherein in the mounting step, the substrate is heat treated (see claims 38 and 47); and/or wherein in the block molding step, a peripheral space of the cavity is provided between the plurality of product forming areas and the air vent, with a width of the peripheral space being larger than a width of spaces between the plurality of the product forming areas in plan view (see claim 39).

The present invention is directed to a technique particularly suitable for manufacture of semiconductor devices using block molding by transfer molding (e.g., injecting resin into a mold cavity). In the manufacture of semiconductor devices, one technique is to mount a plurality of semiconductor chips on a main surface of a substrate, block-molding the mounted semiconductor chips on the substrate with one resin enclosure, by injection molding, and then separating the plurality of semiconductor chips from each other by cutting the resin enclosure and the substrate into respective devices (thus, for example, a single semiconductor chip or stacked semiconductor chips within each respective package is formed).

A second technique, involving a different technology having different problems and different solutions, includes a potting method. For example, in potting, a problem arises in that air bubbles form in the potted enclosure; however, in such potting, the air bubbles can be removed by placing semiconductor devices, that are in a state in which the resin has not been cured, in a low-pressure atmosphere after potting. In transfer molding, resin injection and curing are performed inside a cavity, and thus the method

for reducing voids by vacuum defoaming, which can be used in a potting method, cannot be adopted.

Due to the different technologies involved, different methods must be used for preventing problems (for example, preventing voids) therein. Note paragraph [0013] on page 6 of Applicants' Substitute Specification. In connection with using block molding by transfer or injection molding, and as found and investigated by the Applicants, and as shown in Figs. 23A to 26B and described in the corresponding description in paragraphs [0004] to [0009] on pages 2-4 of Applicants' Substitute Specification, there arises a specific problem when block transfer molding is used in forming a plurality of semiconductor devices in one resin enclosure. It is emphasized that this problem occurs in block transfer molding, and that there is no disclosure that such problem occurs in potting molding. In performing the block molding by injecting resin into a cavity, the flow of the resin 67A (note the aforementioned Figs. 23A to 26B) along the main surface of the semiconductor chip 61 is resisted by the semiconductor chip. Therefore, the resin formed along the main surface of the chip runs slower than the resin 67A flowing along the side surfaces of the semiconductor chip (see Figs. 24A and 24B). For these reasons, voids 67B tend to be generated at positions where the resin 67A flowing along the main surface of the semiconductor chip 61 meets the resin 67A flowing along the side surfaces of the semiconductor chip 61 (see Figs. 25A and 25B). Particularly troublesome are voids 67C remaining at positions hiding behind the semiconductor chips 61 with respect to the injecting direction S of the resin 67A (see Figs. 26A and 26B). These voids, e.g., voids 67C, are a factor that reduces yield of semiconductor devices.

This problem of voids is even greater when a great amount of filler (for example, 80% or more) is added to the molding resin, e.g., for purposes of reducing warpage due to the shrinkage of the molding resin, to facilitate the dicing process, or for providing a more compatible thermal expansion coefficient of the resin to that of the semiconductor chip. That is, in including a large amount of filler, a thixotropic property cannot be used to remove/avoid voids.

Against this background, the present inventors turned their attention to the wettability of the resin 67A to the main surface of the substrate, and based thereon, have achieved the present invention which overcomes problems of voids, especially in connection with block molding by injection of resin into die cavities. Note paragraph [0014] on page 6 of Applicants' Substitute Specification. That is, Applicants have found that voids in the resin, arising during the block transfer molding by injection of resin, becomes more easily removed from a main surface of a substrate in the step of transfer molding, by performing a plasma treatment, the plasma treatment enhancing wettability of the resin to the main surface of the substrate, e.g., by cleaning the substrate and roughening the substrate, after mounting the semiconductor chips on the substrate.

That is, as described, for example, from paragraph [0067] through paragraph [0070] on pages 18-20 of Applicants' Substitute Specification, during the mounting procedure the substrate is heated and impurities such as fats, oils and organic solvents are outgassed so as to contaminate the main surface of the substrate. Performing the plasma treatment removes impurities, such as fats and oils; and, moreover, can roughen the surface of the substrate, all increasing wettability thereof. Since these

impurities have been removed, the resin from along the side surfaces of the semiconductor chip 10 is allowed to easily enter positions, e.g., behind the semiconductor chips with respect to the injecting direction S of the resin 24A (see, e.g., Figs. 14A and 14B of Applicants' disclosure). As a result, the voids 24B generated at the positions where the resin 24A flowing along the main surface of the semiconductor chip 10 meets the resin 24A flowing along the side surfaces of the semiconductor chip 10 are dislodged, and the voids thus dislodged are able to easily move in response to the flow of the resin in the resin injecting process. Therefor, the voids do not remain at positions behind the chips, and, thus, problems due to such voids can be avoided.

Tsuruta discloses a process for molding semiconductor chips, and a molding die used therein. The process includes steps of preparing a circuit panel having plural conductive patterns formed on an insulating layer and plural semiconductor chips mounted on the circuit panel and electrically connected to the plurality conductive pattern, respectively; accommodating the semiconductor chips mounted on the circuit panel in a cavity of a molding die having a gate extending along one of peripheral lines defining the cavity; supplying melted synthetic resin through the gate into the cavity so as to fill the vacant space of the cavity therewith; solidifying the melted synthetic resin; and cutting the large piece of synthetic resin so that the semiconductor chips are sealed in small pieces of synthetic resin, respectively. See column 3, lines 29-45. Looking to Figs. 4 and 5, and the description in connection therewith in columns 5 and 6, this patent discloses dummy cavity 21g in parallel to the gate 21b; the dummy cavity 21g is effective against wire weep and voids, in that resin injected from the gate 21b

falls into dummy cavity 21g so that synthetic resin in cavity 23 is not subjected to turbulence.

It is respectfully submitted that this patent does not disclose, nor would have suggested, the problem addressed by Applicants, of voids in sealing resin formed by block molding a plurality of chips within a single resin block which is later cut, due to flow of resin along the chips, and particularly voids formed behind chips in the direction of resin flow; and would have neither disclosed nor would have suggested the solution to this problem of voids as discovered by Applicants, of conducting the plasma treatment after mounting and prior to block molding; or the particular molding die used.

In particular, it is emphasized that Tsuruta requires the dummy cavity, and it is respectfully submitted that this reference does not disclose, nor would have suggested, the air vent as in claim 29, much less the air vents as in claims 55, 56, 59 and 60. In this regard, note that Tsuruta, in plan view, does not even show the end sides of the molding die. Clearly, Tsuruta is not concerned with any air vent structure, and does not disclose, nor would have suggested, use of the molding die as in the present claims, having the recited air vent as in claim 29, and especially having the structure of air vents in sides of the cavity as in claims 55, 56, 59 and 60.

Moreover, clearly Tsuruta does not disclose, nor would have suggested, the plasma treatment after the mounting step, and prior to the block molding by injecting resin, and advantages thereof, especially in solving the problem addressed by the present invention. In this regard, it is again emphasized that Tsuruta does not disclose, nor would have suggested, the problem addressed by the present invention, of voids due to differential flow of resin at the semiconductor chips, nor would have disclosed or

suggested the solution of this problem. Again emphasizing that the present invention as a whole must be considered, including the problem addressed and solved, and source of this problem, clearly the teachings of Tsuruta are deficient with respect to the presently claimed subject matter.

It is respectfully submitted that the additional teachings of Hashimoto would not have rectified the deficiencies of Tsuruta, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Hashimoto discloses a method of manufacturing electronic parts, including a substrate manufacturing step for forming through holes in a substrate material along lattice-like imaginary lines, the through holes being caused to have external electrodes formed by cutting the through holes along centers thereof; a mounting step for mounting element parts in regions of the substrate material surrounded by the imaginary lines; a connection step for establishing electrical connecting among the element parts and the corresponding through holes; a molding step for introducing molding resin into the entire surface of the substrate material to mold the element parts; and a cutting step for cutting the substrate material, the molding resin and the through holes along the imaginary lines after the molding resin has been hardened. See column 3, lines 41-55. Note also column 4, lines 33-43, disclosing use of a closing member for closing an opening portion of each of the through holes prior to performing the molding step, and an opening step for removing the closing member after the molding resin has been hardened. This patent further discloses injection of conductive paste, e.g., solder paste, into the through holes, to fill the through holes with solder. See column 9, lines 24-45. Column 15, lines 3-20, of this patent discloses that if

potting molding is employed, generation of portions that are not filled with molding resin 5 can be prevented completely by performing vacuum defoaming in the process for applying the molding resin; and that when using potting molding, if the surfaces of the substrate 6 and the semiconductor device 1 are activated with oxygen or argon plasma immediately before the process for applying the molding resin 5, further excellent contact of the molding resin 5 can be established.

It is emphasized that the disclosure of activation with oxygen or argon plasma immediately before the process for applying the molding resin is disclosed where the potting molding is employed. It is respectfully submitted that this disclosure in Hashimoto, in connection with potting molding, would not have been properly combinable with the teachings of Tsuruta, as applied by the Examiner. That is, it is respectfully submitted that the teachings of Tsuruta and of Hashimoto, applied by the Examiner, are directed to non-analogous art. In this regard, it is respectfully submitted that the injection molding process of Tsuruta is a different technological process than the potting molding of Hashimoto, having different problems in connection with each, and it is respectfully submitted that, accordingly, these references are directed to non-analogous arts.

During the aforementioned interview, the Examiner emphasized that both Tsuruta and Hashimoto are directed to forming packaged semiconductor devices, and thus the teachings of these patents are analogous. However, the Examiner is respectfully reminded that the present claims, as well as the teachings of Tsuruta and of Hashimoto as applied, are directed to methods; and it is respectfully submitted that notwithstanding that each of Tsuruta and Hashimoto form a packaged semiconductor

device, the processes described in each are not analogous.

That the processes described in the two references are not analogous is supported by the specification of the above-identified application, in particular, the description in paragraph [0013] on page 6 of Applicants' Substitute Specification. Thus, it can be seen that a defoaming technique can be used in a potting method to avoid voids, which technique cannot be used for overcoming voids in the injection molding. This shows that injection molding and potting molding are different technologies at the heart of a void problem, such that the techniques are clearly non-analogous.

It is again emphasized that the problem addressed by Applicants and solved by Applicants are voids in the resin, and Applicants have found a source of this problem upon turning their attention to the wettability of the resin 67A to the main surface of the substrate 60. See paragraph [0014] on page 6 of Applicants' Substitute Specification. That is, Applicants turned their attention to the wettability, and their findings in connection with wettability to develop a technique to avoid voids, forms part of the present invention as a whole. In view thereof, it is respectfully submitted that Applicants have found a source of the void problem; and based thereon, have found a solution thereto. Taking this discovery of the source and of the solution as part of the present invention as a whole, it is respectfully submitted that the teachings of the applied prior art, even taken as a whole, would have neither disclosed the source of the voids problem, and solution thereto, as in the present invention.

In addition, it is respectfully submitted that the Examiner has not established motivation for combining the teachings of Tsuruta and of Hashimoto, as applied by the

Examiner. Particularly in view of the different technologies involved in Tsuruta and in Hashimoto, and different problems addressed by each, it is respectfully submitted that one of ordinary skill in the art concerned with in Tsuruta, utilizing injection molding and attempting to prevent the molded product from voids and a wire weep, would not have looked to the teachings of potting molding as in Hashimoto.

Furthermore, even assuming, arguendo, that the teachings of Tsuruta and of Hashimoto were properly combinable, it is respectfully submitted that such combined teachings would have neither disclosed nor would have suggested the present invention, including the plasma treatment. In this regard, it is emphasized that Hashimoto merely discloses that if the potting molding is employed, and if the surfaces of the substrate 6 and the semiconductor device 1 are activated with oxygen or argon plasma immediately before the process for employing the molding resin is performed, further excellent contact of the molding resin 5 can be established. This patent only discloses activation with oxygen or argon plasma, in connection with potting molding. It is respectfully submitted that the teachings of this patent, even in combination with the teachings of Tsuruta, would have neither disclosed nor would have suggested treatment with an oxygen or argon plasma after the mounting step and prior to arranging the substrate in the molding die, particularly wherein impurities remaining on the main surface of the substrate are removed or the main surface of the substrate is roughened, and especially wherein the plasma treatment is performed to provide a function as in various of the present claims (see, e.g., claims 49-51, 57, 58, 61 and 62).

In the paragraph bridging pages 2 and 3 of the Office Action mailed

June 9, 2003, the Examiner quotes from column 15, lines 14-20 of Hashimoto. It is respectfully submitted that this shows that the Examiner is, improperly, looking at bits and pieces of Hashimoto, without taking the teachings of this reference as a whole as required under 35 USC §103. That is, the quoted portion of Hashimoto is only applicable if the potting molding is employed, as is clear from column 15, line 3 of Hashimoto. Taking the teachings of Hashimoto as a whole, it is respectfully submitted that this reference only teaches "activation" of surfaces of the substrate and the semiconductor device 1 with oxygen or argon plasma immediately before the process for applying the molding resin 5 is performed, to achieve further contact of the molding resin, where potting molding is employed; and it is respectfully submitted that the teachings of Hashimoto, even in combination with the teachings of Tsuruta, would have neither taught nor would have suggested application of oxygen or argon plasma treatment at the time of treatment as in the present claims, particularly avoiding the problems, and sources thereof, as found and addressed by Applicants.

The contention by the Examiner that roughening and impurity removal are inherent aspects of the plasma treatment process, is noted. It must be emphasized, however, that Hashimoto discloses oxygen or argon plasma treatment "for activation"; it is respectfully submitted that this disclosure does not teach, nor would have suggested, "inherent" impurity removal and roughening as alleged by the Examiner.

In the Office Action mailed June 9, 2003, the Examiner has not even addressed the issues of the present invention as in previously considered claims 49-51. Note also presently submitted claims 55, 56, 59 and 60. Clearly, the teachings of Tsuruta and of Hashimoto, even if properly combinable, would have neither taught nor would have

suggested the aspects of the present invention wherein the treating step by plasma is performed to increase wettability so as to provide the function as in each of claims 49-51; or wherein sufficient plasma treatment is performed so as to achieve the function as in claims 57, 58, 61 and 62.

It is respectfully submitted that the additional teachings of Ishikawa would not have rectified the deficiencies of Tsuruta and of Hashimoto, even if these teachings were properly combinable, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Ishikawa discloses a resin-mold type semiconductor device packaged with an epoxy-based resin, and a manufacturing method therefor. The method includes steps of supporting and fixing a semiconductor chip on a die pad; electrically connecting distal end portions of a plurality of inner leads which face the semiconductor chip to a plurality of terminal electrodes of the semiconductor chip by bonding wires, respectively; molding the die pad, the semiconductor chip, the plurality of inner leads and the bonding wires in a resin mold which is made of a sealing resin; and forming highly water-absorbent insulating film made of a highly water-absorbent polymer on a surface of the resin mold. See column 3, lines 50-63. In column 6, lines 60-67, the sealing resin is disclosed as an epoxy resin containing a silica filler in an amount of 70-80% by weight based on the overall weight of the resin-mold package.

Even assuming, arguendo, that the teachings of Ishikawa were properly combinable with the teachings of the other references as applied by the Examiner, it is respectfully submitted that such combined teachings would have neither disclosed nor would have suggested the void problem which is especially severe when using a

sealing resin containing relatively large amounts of filler; and would have neither taught nor would have suggested the presently claimed invention, including addressing wettability as a source of the void problem and solving such problem by the plasma treatment, especially together with the molding die used.

In view of the foregoing comments and amendments, particularly together with the concurrently filed RCE Transmittal, withdrawal of the finality of the Office Action mailed June 9, 2003, and entry of the present amendments, and reconsideration and allowance of all claims remaining in the application, are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.40695X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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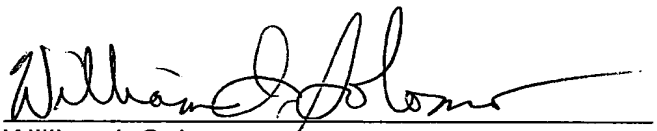

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